



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

**SUBMITTAL OF FORMAL DRAWINGS**

APPLICANT: Gerald DEBOY et al. GROUP ART UNIT: 2815  
SERIAL NO.: 09/530,553 EXAMINER: P. Brock II  
FILING DATE: July 21, 2000  
INVENTION: HIGH VOLTAGE RESISTANT EDGE STRUCTURE FOR  
SEMICONDUCTOR COMPONENTS

Hon. Assistant Commissioner for Patents  
Washington D.C. 20231

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2800 MAIL ROOM

SIR:

Enclosed herewith is two sheets of formal drawings showing Figure 1 and Figures 4A - 4D. The formal drawings incorporate the changes approved by the Examiner. Acceptance of the formal drawings is hereby requested.

Respectfully submitted,

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CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to:

The Assistant Commissioner for Patents  
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on October 29, 2002.